REMARKS

No New Issue is Raised. The presently-requested amendment adds the subject matter of two respective dependent claims to each of the independent claims (e.g., 2 and 7 are combined into 1). The combination of an independent with *two* dependent claims, both of which had depended directly from the independent claim, does not require additional consideration by the Examiner. The reason is that the three-way combined claim is allowable if *either* of the previous dependent claims were allowable. For example, if the Examiner is convinced that former claim 2 would now be allowable by the Applicant's present arguments, then amended claim 1 can be allowed without consideration of the subject matter of former claim 7 (which can only make the combination of claims 1and 2 narrower).

The combination of (for example) claims 1, 2, and 7 has the same relation to a combination of claims 1 and 2 as a dependent claim has to a base claim, and a dependent claim is always allowable if the base claim is allowable, so that the dependent claim requires no additional consideration. Therefore, the combination of claims 1, 2, and 7 is allowable if the combination of claims 1 and 2 is allowable (or, if the combination of claims 1 and 7 is allowable).

Because of this, no additional consideration is required of the Examiner if this amendment is entered, as claims 2 and 7 were already pending individually. Therefore, entry is proper.

In response to the outstanding Office action:

[1-2] Claims 1 and 9 were rejected under §103(a) as being unpatentable over Bulucea '701 in view of Chen '517. This rejection is respectfully traversed.

Bulucea. Bulucea discloses (see Figs. 15-16) a channel region of n-doped material 110 and source and drain 112, 114 of more heavily-doped n++ material. All of these sit atop some p-doped material 106, which in turn sits on progressively positively-doped materials 104 (p+) and 102 (p++). Adjacent devices are separated by insulation 108 (col. 35, lines 1-10) made of field oxide (col. 37, line 30), but there is no insulation between the upper n-doped materials of the source, drain, and channel and the lower p-doped region (applied Fig. 16). The structure shown in applied Fig. 16 is a "complementary-CJIGFET structure" (col. 37, line 15).

"CJIGFET" is Bulucea's term for an insulated-gate FET or IGFET (col. 1, line 16) which has a channel, source, and drain of the same conductivity type (col. 2, line 48 and col. 2, line 66 to col. 3, line 5). The "complementary" version of this device, which is shown in Fig. 16, has two transistors of opposite polarities (col. 3, lines 11-13).

16 shows that Bulucea provides a base of material complementary to the channel, source, and drain. For the n-type structure 112, 114, 116 on the left side of Fig. 16, there is a p-type base 106; on the right, an n-type base 166 underlies the p-type structure 170, 172, 174. The basic idea of this arrangement is explained on drawing sheet 1, which shows how the voltage V_G at the uppermost electrode changes the depletion region 44. The Examiner is invited to note Fig. 2, which shows how the doping changes with height in the structure of Figs. 1a and 1b: from p in the channel to n below (col. 12, lines 1-12).

The doping scheme of Fig. 2, which creates a pn junction, is important to Bulucea's theory and to the transistor shown in applied Fig. 16. Starting at col. 13, line 18, Bulucea explains in detail how this structure works. For example, col. 14, line 34, explains that "y_{JMIN} is the thickness of the channel-side portion of the depletion region 44 ... and thus is the minimum junction depth for buried-channel operation. In order to determine channel-side channel/body depletion thickness y_{JMIN}, the center dopant profile of FIG. 2 is ... at uniform value N_B across ... body region 22." The dopant quantity N_B occurs in equations 9, 10, 24, 25, 29, 34-40, 42, 44, 46,

49, 50-51 (as an averaged quantity N_B^{-m}, see col. 9, line 58), and 69, and also in the un-numbered equation in claim 13. The related quantity N_{B0} (background dopant concentration, see col. 9, line 55) appears in several other equations.

Clearly, the doping N_B of the region 22 is an important aspect of the theory and construction of Bulucea's Fig. 16 transistor. Figs. 15-16 , which show the preferred embodiment, and come directly after the theoretical section of the description and embody that theory.

By disclosing that the underlying layers 106, 166 of Fig. 16 are important to the functioning of its invention, Bulucea inherently teaches against removing them, altering them, or interposing anything between them and the upper layers (such as an un-doped silicon layer that would destroy the pn junction Bulucea has so carefully calculated).

Motivation. Chen is applied for teaching the addition of the SOI layer that is lacking in Bulucea. The Examiner states that the SOI layer would prevent electrical interference from adjacent devices (page 3, line 1).

However, Bulucea *already* has an insulator to separate and isolate the transistors, namely, field-oxide region 108 which "separates the device region for CJIGFET 100 from other such active device regions" (col. 35, line 8). With respect, Bulucea needs no other insulation layer to prevent interference, contrary to the motivation proposed by the Examiner.

The Opposite of Insulation. Furthermore, no insulating layer is provided anywhere *under* the applied transistor of Bulucea. The layer 124 of Fig. 16 is metallic (col. 38, line 59). Thus, in the region under the channel, Bulucea provides not an insulating layer, but the opposite—a metallic conducting layer.

There Is No Expectation of Success. Chen discloses that its uppermost SOI layer 16 is the portion in which IC devices will be formed (col. 3, line 20), but there is no explanation whatsoever of what or how the IC devices are formed. Chen is concerned only with gettering to remove metals from the SOI (col. 1, lines 28-43; col. 5, lines 33-40), which appears to the

Applicant to be a step prior to forming any ICs. The region under the gate electrode 20 and gate stack 22 is shielded, and is not gettered.

If Bulucea were subjected to the gettering of Chen, then the entire structure would be destroyed, since the n++ or p++ source/drain areas 112, 114, 172, 174 would become un-doped by Chen's gettering argon, helium, or germanium atoms 26 (Fig. 3; col. 5, line 38). Therefore, the teachings of Chen would not have been combined with the Bulucea.

[3] Claims 2, 3, 10, and 11 were rejected under §103(a) as being unpatentable over Bulucea and Chen in view of Tsukii '858, previously applied. This rejection is respectfully traversed. (Claim 2 is now included in claim 1 and claim 10 in claim 9.)

(1) The Examiner asserts obviousness based on making Bulucea's structure applicable in an integrated circuit structure like that of Tsukii. This is respectfully traversed on the basis that Bulucea *already* shows an integrated circuit in applied Fig. 16, with complementary n-p and p-n transistors formed on a single substrate. (Two transistors on one substrate is believed to define an integrated circuit.) The asserted motivation is, with respect, obviated.

(2) Furthermore, Bulucea goes to great lengths to calculate based on an optimum channel doping concentration N_C (col. 9, line 60). Concentration N_C appears in equations 9-11, 16, 17, 19, 20, 22, 24, 25, etc. The person of ordinary skill would not have throw away Bulucea's carefully and fully theorized values of N_C due to the mere mention of some other concentration in a reference like Tsukii, that is not directly related to Bulucea's structure and does not contain any explicit teaching of the advantage of its particular concentration.

[4] Claims 4, 5, 12, and 13 were rejected under §103(a) as being unpatentable over Bulucea and Chen in view of Stein '787, previously applied. This rejection is respectfully traversed on the basis of the arguments above and the dependence of these claims.

[5] Claims 6 and 14 were rejected under §103(a) as being unpatentable over Bulucea and Chen in view of Yamada '070, previously applied. This rejection is respectfully traversed on the basis of the arguments above and the dependence of these claims.

[6] Claims 7, 8, 15, and 16 were rejected under §103(a) as being unpatentable over Bulucea and Chen in view of Kato '678, previously applied. This rejection is respectfully traversed.

(1) Kato states that the 0.15 μm length disclosed at col. 2, line 5 (applied in the rejection) makes it "difficult that the high integration memory device of 256 mega bits or more be realized" (col. 2, line 6). Thus, Kato teaches *away* from using this length and the person of ordinary skill in the art would never have combined the references based on this teaching.

(2) Bulucea is greatly concerned with channel depth, but completely ignores channel *length*; all of its figures show channel cross sections, and no variable for channel length appears in its long list of variables (col. 9, line 31 to col. 11, line 35). Why?

The Applicant believes that Bulucea is aware that the properties of its structure can be extended to a desired length, knows that the person skilled in the art would also be aware of this, and therefore provides no discussion of the length. An electrical analogy to Bulucea would be a theoretical discussion of a coaxial cable structure given and discussed only in cross section; the properties of any length of such coaxial cable would evident to the person skilled in the art of coaxial cables.

Thus, any teaching of Kato about length is seen to be irrelevant to the teachings of Bulucea.

In summary, the Applicant sees no motivation to combine the references.

Entry of this Amendment and withdrawal of the rejections is requested.

Respectfully submitted,

October 18, 2005
Date

Nick Bromer (Reg. No. 33,478)
(717) 426-1664
RABIN & BERDO, P.C.
CUSTOMER NO. 23995
Telephone: (202) 371-8976
Telefax : (202) 408-0924